

# Design of a Multi-Channel Pre-Beamform Data Acquisition System for an Ultrasound Research Scanner

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**Abstract**—Access to the pre-beamform data of each array channel on an ultrasound scanner is important to experimental investigations on advanced imaging research topics like adaptive beamforming and synthetic aperture imaging. Through such data access, we can obtain in-vitro or in-vivo insights on various imaging methods without resorting to hardware implementation. This paper reports the development of a pre-beamform data acquisition (DAQ) system that can collect data from 128 array elements in parallel. Our DAQ system is intended to interface with a Sonix-RP research scanner through a probe connector port. It comprises three major blocks: 1) a connector board that interfaces with the array probe and the scanner; 2) a main board that triggers data acquisition and controls data transfer to a computer; 3) four receiver boards that are each responsible for acquiring 32 channels of digitized raw data and storing them to the on-board DDR2 memory. The probe-connecting end of this system is interfaced with TX810 chips to facilitate switching between transmit and receive modes. When receiving data, the incoming analog signal is first passed into a low-noise amplifier. These signals are then sent into AD9272 chips on the four receiver boards to perform time gain compensation, anti-alias filtering, and 12-bit data sampling at an 80MHz rate. Subsequently, the digitized signal samples are de-serialized using a Virtex-5 FPGA and are stored into DDR2 memory. To facilitate data retrieval, we implemented a Virtex-5 FPGA on the main board to initiate data transfer, and if preferred, to perform on-board beamforming (programmable by user) prior to sending data to a computer through a USB 2.0 link. For our prototype, we used 16GB of DDR2 memory for data storage. With a frame rate of 35Hz, a 10cm depth-of-view and 128 transmit firings per frame, this DAQ system is capable of collecting pre-beamform data from all array channels for 2.5 seconds. We are currently completing the prototype development in collaboration with Ultrasonix.

**Keywords**—pre-beamform data, multi-channel data acquisition, system hardware design.

## I. INTRODUCTION

In ultrasound imaging research, access to the raw scanner data used for image formation is essential to carry out experimental investigations of new methods and algorithms.

Through such data access, researchers can obtain in-vitro or in-vivo insights on various imaging methods without resorting to hardware implementation that is often costly and time-consuming [1]. To address this research need, some groups have developed data acquisition (DAQ) interfaces in the form of add-ons designed specifically for clinical ultrasound scanners. For instance, Ashfaq et al. [2] have implemented an add-on DAQ tool for the Siemens Antares system, while Shamdasani et al. [3] have developed one that interfaces with a Hitachi HiVision scanner. Other imaging researchers have met their data access needs either by purchasing an open-architecture scanner available on the market [4] or by designing their own in-house systems [5], [6]. For these research interfaces or scanners, raw ultrasound data is considered as the ones sampled after beamforming, which is an upstream processing step that influences the imaging resolution. Whilst access to the post-beamforming ultrasound data is important for evaluation of new signal processing methods such as adaptive color Doppler clutter filtering [7], it does not support studies on next-generation imaging paradigms like synthetic aperture imaging [8], adaptive beamforming [9], and photoacoustic imaging [10] that work with the pre-beamform data of each element on the ultrasound array. As such, the development of a pre-beamform DAQ tool is necessary to serve frontier research efforts in ultrasound imaging.

A few groups have reported the design of pre-beamform DAQ tools for advanced ultrasound imaging studies. For instance, Fabien et al. [11] have described an add-on hardware that can acquire pre-beamform data from a Philips SONOS-5500 scanner. As well, Jensen et al. [12] have developed an in-house system to support their group's investigations on synthetic aperture imaging. Recently, Mo et al. [13] have reported an expanded research package that includes pre-beamform DAQ functionality on the ZONARE z.one system.

In this paper, we present the design of a pre-beamform DAQ system that can collect data from a Sonix-RP research scanner (Ultrasonix Medical Corporation, Richmond, BC, Canada) without interrupting the normal operations during a diagnostic scan. Our focus shall be on presenting this DAQ system's design considerations and its overall architecture.

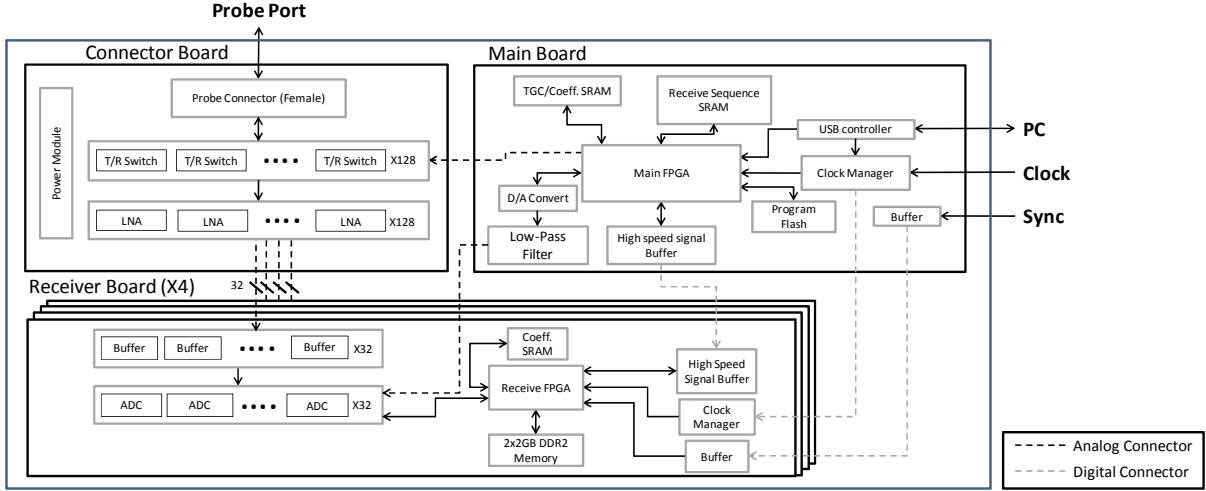


Fig. 1. Overall system architecture of pre-beamform DAQ system. This architecture has been designed to support parallel acquisition of pre-beam-form data in 128 channels from a Sonix-RP scanner.

## II. DESIGN CONSIDERATIONS

### A. System Issues

The purpose of the DAQ system is to acquire and process pre-beamform data for studying advanced ultrasound imaging using a Sonix-RP scanner. To achieve this goal, three major issues have been considered, including:

1) *Interface with Scanner*: The system is intended to serve as a plug-in module for the Sonix-RP scanner and should be able to acquire the data without interrupting the normal operations of the scanner. This would allow the users to locate the region of interest before acquiring the data.

2) *Parallel Data Acquisition*: In demanding applications like synthetic aperture imaging, often a large number of receive elements are activated simultaneously. One of the major considerations of the DAQ system would therefore be its capability of collecting the data from all the receive channels in a parallel and synchronized manner.

3) *Reconfigurability*: In order to help users to pursue different imaging studies, our DAQ design should allow the user to have complete control over the DAQ process. This should be achieved through a FPGA-based design. By re-programming the FPGAs, users can define the DAQ parameters and implement on-board beamforming if desired.

### B. Implementation Issues

In addition to the system-level issues, different aspects related to implementation have also been considered:

1) *Signal Amplification*: In some applications like photoacoustic imaging, the received signal strength would be so weak that the ADCs cannot capture the signals. As such, it may be necessary to use low noise amplifiers (LNAs) so that the system can amplify the receive signals with a large gain.

2) *Sampling Rate*: In typical ultrasound imaging applications, the carrier frequency is usually below 20 MHz.

Hence, deducing from the Nyquist sampling theory, the sampling frequency should be at least 40MHz to prevent aliasing. Also, the sampling rate should be sufficiently high so as to reduce the error caused by applying the delay during beamforming.

3) *Bit Resolution*: Due to issues such as attenuation and noise, the dynamic range for the received signal is quite large, typically about 60 dB. Perhaps a suitable choice would be to use a 12-bit ADC that has a range of 72 dB.

4) *Memory*: Parallel data acquisition would lead to a large data throughput. In addition, in some clinical studies such as cardiac imaging, pre-beamform data over few seconds would be needed. A large memory would then be needed to store all the data. Note that the memory required per second is given by

$$Memory = TOF \times PRF \times f_s \times N_{bl} \times N_{byte}$$

where  $TOF$  is the time of flight,  $PRF$  is the pulse repetition frequency,  $f_s$  is the sampling frequency,  $N_{bl}$  is the no. of beamlines and  $N_{byte}$  is the no. of bytes needed for each sample.

## III. SYSTEM ARCHITECTURE

Given the requirements stated in Sec. II, a multi-channel pre-beamform DAQ system for the Sonix-RP scanner has been developed. This system is a plug-in module which interfaces with the scanner and the array probe (Sec. II-A(1)). As shown in Fig. 1, it comprises 3 major building blocks: a connector board, a main board, and 4 receiver boards. The overall system behaviour is as follows: The probe-connecting end of this system is interfaced with T/R switches to facilitate switching between transmit and receive modes. In the transmit mode, the firing table stored in the receive sequence SRAM is read and the required array channels are activated accordingly (Sec. II-A(2)). In the receive mode, the incoming analog signal is first passed into a LNA (Sec. II-B(1)). These signals are then sent into the ADCs on 4 receiver boards to perform time gain compensation (TGC), anti-alias filtering and 12-bit data

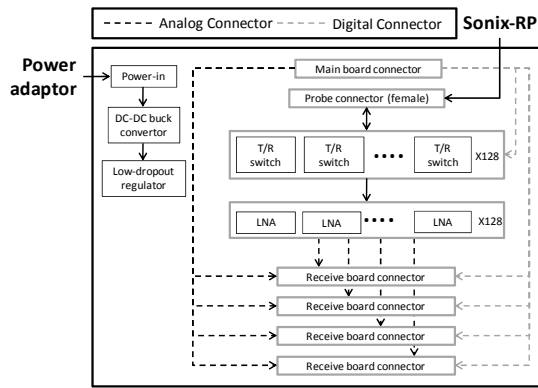


Fig. 2. Connector board: block diagram. This board serves as the interface between the DAQ system, the array probe, and the scanner.

sampling at an 80MHz rate (Sec. II-B(2),(3)). The digitized signal samples are then de-serialized using an FPGA and are stored into DDR2 memory. To facilitate data retrieval, an FPGA is implemented to initiate data transfer, and if preferred, to perform on-board beamforming (programmable by user, see Sec. II-A(3)) prior to sending data to a computer through a USB 2.0 link. For data storage, a total of 16GB DDR2 memory is used. With a frame rate of 35Hz, a 10cm depth-of-view and 128 transmit firings per frame, this DAQ system should thus be capable of collecting pre-beamform data from all array channels for 2.5 seconds (Sec. II-B(4)), which corresponds to 2-3 cardiac cycles.

The functions of each board are discussed in detail in the following sub-sessions:

#### A. Connector Board

The block diagram of the connector board is shown in Fig. 2. It is intended to interface the DAQ system with the array probe and the scanner. The main board and the 4 receiver boards are also connected to this board. There are two different connectors: one for analog signals and the other for digital signals. The functions of the connect board include:

1) *Interfacing with Sonix-RP Scanner*: A 156 pin tyco/cannon male connector is used as the probe connector on the connector board. The DAQ system and the array probe used are plugged into 2 different probe ports of the Sonix-RP scanner and are enabled at the same time. In this way, both of them can function concurrently and the RF signals received by the transducer can be redirected to the DAQ system.

2) *T/R Switching*: These are implemented on the connector board using Texas Instrument IC TX810. It can be programmed by the FPGA on the main board to activate selected channels and toggle between transmit/ receive modes.

3) *Power Supply*: This unit is housed on the connector board to deliver power to the whole system. It provides various voltage inputs to different system components and stabilizes the power supply.

4) *Pre-amplification (optional)*: As an optional function, pre-amplification can be provided to boost the signal intensity

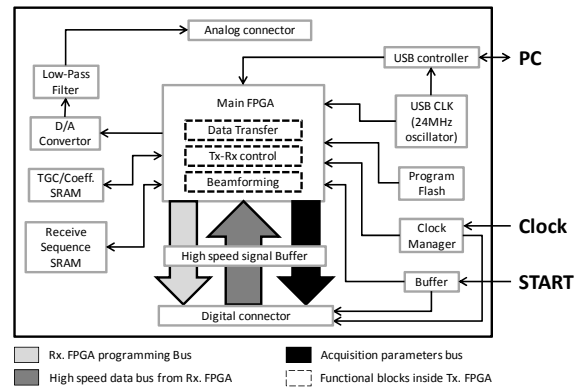


Fig. 3. Main board: block diagram. This board mainly acts as the controller for the DAQ process from the array probe and the USB data transfer process. It also controls TGC parameters and performs on-board beamforming.

of weak signals such as photoacoustic signals by using LNAs implemented with MD3880.

#### B. Main Board

The main board shown in Fig. 3 is responsible for triggering DAQ process and controlling data transfer from/to the computer. The functions of the main board are listed below:

1) *Signal Receive Control*: A T/R controller implemented with a Virtex 5 FPGA on the main board (i.e. the main FPGA) is used to control the RF signal receive process. During operation, the controller reads the receive sequence table stored in the receive sequence SRAM and activates the required receive channels by controlling the T/R switches on the connector board. This table can be modified by user through USB linkage to the downlink PC. Furthermore, the main FPGA synchronizes the data acquisition of all 128 channels by communicating with the receive FPGAs on receiver boards and adjusting the time delays of these 128 channels to compensate for the signal path differences.

2) *TGC Control Signal Generation*: Two TGC modes are available in this system: 1) memory mode and 2) scanner mode, both of which are controlled by the main FPGA. In the memory mode, the main FPGA sends the TGC parameters stored in the TGC SRAM to the VCAs on the receiver boards. The TGC parameters are passed through a D/A convertor on the main board to be converted into analog control signal before being sent to the VCAs. In the scanner mode, the main FPGA passes the TGC parameters used in the Sonix-RP scanner instead.

3) *Beamforming*: On-board beamforming can be performed in this system through the FPGAs. During operation, the main FPGA first sends the channel delay coefficients to the receive FPGAs to perform partial beam summations on individual receiver board. It then receives the results and performs final summation to yield the post-beamform data. Theoretically, the total computational power available is  $1 \times 10^{11}$  flops per second (5 FPGAs with 40 DSP slices @ 500MHz per FPGA). Users can also utilize these resources to design their own beamforming algorithms.

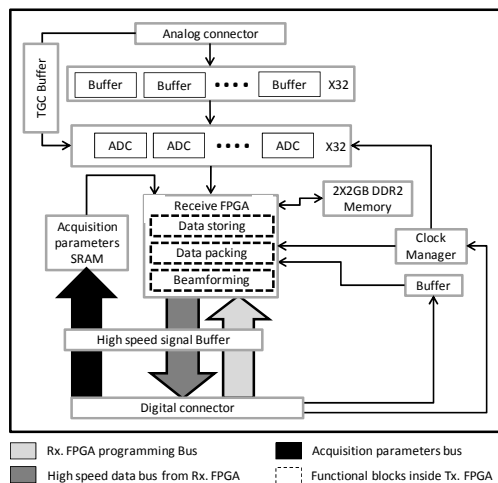


Fig. 4. Receiver board: block diagram. Each board performs pre-beamform DAQ for 32 channels and stores the samples in a 4GB RAM. It also amplifies, filters, and applies TGC to the analog signals. Partial on-board beamforming can be carried out as well.

4) *USB Communication*: An USB controller (CY7C6801 USB microcontroller) is installed on the main board to facilitate the data transfer between the DAQ system and the downlink PC. Apart from acquiring the received data to the PC, it is used to program the FPGAs on both the main board and receiver boards and send the parameters to the SRAMs.

### C. Receiver Boards

As shown in Fig. 4, each receiver board is responsible for acquiring 32 channels of digitized raw data and storing them to the on-board DDR2 memory. Their functions include:

1) *Pre-amplification (optional)*: A second set of LNAs inside the ADC chips AD9272 are provided to amplify weak signals in addition to the set provided on the connector board.

2) *Filtering*: There are two analog filters on each receive board: an anti-aliasing filter and a DC-cutoff filter. They are implemented with programmable filters in AD 9272.

3) *Time Gain Compensation (TGC)*: TGC is performed to compensate for signal drop due to attenuation. It is achieved by using the VCAs inside AD 9272. The gain of the VCAs is controlled by the TGC control signal generated by the main FPGA on the main board as discussed in session III-B.

4) *Analog to Digital Conversion*: After the filtering and amplification stages, the analog ultrasound signals are digitalized and transmitted in the form of LVDS by the AD 9272 with a 12-bit resolution at 80MHz sampling rate.

5) *Data Processing and Storage*: The receive FPGA on each receiver board de-serializes the LVDS inputs from the ADCs. Two 12-bit data and an 8-bit cyclic redundancy check code are packed together to form a 32-bit data which is stored in the 4GB DDR2 RAM (16GB in total for 4 receiver boards). DDR2 RAM is chosen due to its high read/ write speed.

6) *Beamforming*: As mentioned in session III-B, each receiver board is required to perform partial beam summation

of the 32-channel data with proper delays. The results from all 4 boards are sent to the main FPGA for final computation.

## IV. CONCLUDING REMARKS

The first prototype of the DAQ system is now under fabrication in collaboration with Ultrasonix. The system should be able to acquire pre-beamform data from 128 array elements in parallel and is intended to interface with a Sonix-RP research scanner. The reconfigurability of the system also allows the implementation of user-defined functions. It is our hope that, by designing a DAQ system for a widely used research scanner, we can help ultrasound imaging researchers gain access to pre-beamform data required to pursue in-vitro and in-vivo evaluation of advanced ultrasound imaging paradigms such as synthetic aperture imaging and photoacoustic imaging.

## ACKNOWLEDGEMENTS

We like to express our deepest gratitude to Kris Dickie and colleagues at Ultrasonix for their technical support. We also like to thank Prof. Paul Cheung for his ongoing advice.

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